OPTOELECTRONIC SEMICONDUCTOR PACKAGE DEVICE

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part of U.S. Application Serial No. 10/042,812 filed January 9, 2002, which is incorporated by reference.

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor packaging, and more particularly to

10   optoelectronic semiconductor package devices.

Description of the Related Art

In the field of electronic systems, there is a continuous need to increase performance and reduce size. This is largely achieved by improving semiconductor wafer manufacturing and

15   semiconductor packaging technologies. Wafer manufacturing involves simultaneously fabricating numerous semiconductor chips as a batch on a silicon wafer using various etching, doping and depositing steps. After the wafer is complete, the chips are separated from one another and packaged.

Wafer manufacturing strives to reduce transistor or capacitor feature size in order to

20   increase circuit density and enhance functionality. Device geometries with sub-micron line widths are so common that individual chips routinely contain millions of electronic devices. Reduced feature size has been quite successful in improving electronic systems, and continuous development is expected in the future. However, significant obstacles to further reduction in feature size are being encountered. These obstacles include defect density control, optical system

25   resolution limits, and availability of processing material and equipment. Attention has therefore increasingly shifted to semiconductor packaging as a means to fulfill the relentless demands for enhanced system performance.

Semiconductor chips have input/output pads that must be connected to external circuitry in order to function as part of an electronic system. Traditionally, a single chip is individually

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housed in a single-chip package that is connected to other single-chip packages through a printed circuit board (or motherboard) which supplies power to the chips and provides signal routing among the chips. The single-chip package has connection media that is typically an array of metallic leads (e.g., a lead frame) or a support circuit (e.g., a substrate).

5   Several connection techniques are widely used for connecting the chip pads and the connection media. These include wire bonding, tape automated bonding (TAB) and flip-chip bonding. Wire bonding is by far the most common. In this approach, wires are bonded, one at a time, from the chip to external circuitry by thermocompression, thermosonic or ultrasonic processes. TAB involves bonding gold-bumped pads on the chip to external circuitry on a

10   polymer tape using thermocompression bonding. TAB requires mechanical force such as pressure or a burst of ultrasonic vibration and elevated temperature to accomplish metallurgical welding between the wires or bumps and the designated surface. Flip-chip bonding involves providing pre-formed solder bumps on the pads, flipping the chip so that the pads face down and are aligned with and contact matching bond sites, and melting the solder bumps to wet the pads

15   and the bond sites. After the solder reflows it is cooled down and solidified to form solder joints between the pads and the bond sites. Many variations exist on these basic methods.

A major advantage of flip-chip bonding over wiring bonding and TAB is that it provides shorter connection paths between the chip and the external circuitry, and therefore has better electrical characteristics such as less inductive noise, cross-talk, propagation delay and waveform

20   distortion. In addition, flip-chip bonding requires minimal mounting area and weight which results in overall cost saving since no extra packaging and less circuit board space are used. While flip-chip technology has tremendous advantages over wire bonding and TAB, its cost and technical limitations are significant. For instance, the cost of forming bumps on the pads is significant. An adhesive is normally underfilled between the chip and the support circuit to

25   reduce stress on the solder joints due to thermal mismatch between the chip and the support circuit, and the underfilling process increases both manufacturing complexity and cost. The solder joints exhibit increased electrical resistance as well as cracks and voids over time due to fatigue from thermo-mechanical stresses. Further, the solder is typically a tin-lead alloy and lead-based materials are becoming far less popular due to environmental concerns over disposing

30   of toxic materials and leaching of toxic materials into ground water supplies. Thus, none of these conventional connection techniques are entirely satisfactory.

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Optoelectronics pertains to the interaction of optical processes with electronic processes. This interaction is typically associated with energy conversion between optical signals and electrical signals. Optoelectronic devices such as lasers, photodetectors, optical modulators, optical switches and optical sensors are examples of devices within which this interaction takes

5   place.

Optical sensors (also called optical detectors or image sensors) have proliferated in a variety of devices that are available both to high-end users, such as professional video studios and graphics art houses, and ordinary consumers as well. Such devices include video cameras, digital still cameras, desktop scanners, film scanners, machine vision equipment, bar-code

10   readers, toys, and biometric tools such as retina, fingerprint, palm and facial recognition scanners that capture relatively high resolution monochrome or color images and convert them into analog or digital signals for storage, manipulation and/or distribution.

Optoelectronic packages for optical sensors often include a chip carrier, an optoelectronic chip mounted in a cavity of the chip carrier, and a transparent window positioned above the chip

15   that hermetically seals the cavity and exposes the chip to the incident light. The optoelectronic chip typically includes a light sensitive cell that comprises an array of tiny photosensor elements, such as charge coupled devices (CCDs) or complimentary metal oxide semiconductor (CMOS) photoreceptors. The photosensor elements convert the light energy incident upon them into electrical signals on an element-by-element or pixel-by-pixel basis. These signals convey

20   information about the intensity, color, hue, saturation and other attributes of the incident light.

Optoelectronic packages with optical windows provided by glass or quartz inserts are relatively expensive to fabricate. Moreover, optoelectronic packages often employ wire bonding, TAB or flip-chip bonding to connect the chip pads to the chip carrier, and as mentioned above, none of these chip pad connection techniques are entirely satisfactory.

25   In view of the various development stages and limitations in currently available optoelectronic semiconductor package devices, there is a need for an optoelectronic semiconductor package device that is cost-effective, reliable, manufacturable, and provides excellent mechanical and electrical performance.

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SUMMARY OF THE INVENTION

An object of the present invention is to provide an optoelectronic semiconductor package device that provides a low cost, high performance, high reliability package.

In accordance with one aspect of the invention, an optoelectronic semiconductor package device includes a semiconductor chip, an insulative housing and a conductive trace, wherein the chip includes an upper surface and a lower surface, the upper surface includes a light sensitive cell and a conductive pad, the insulative housing includes a first single-piece non-transparent insulative housing portion that contacts the lower surface and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, and the conductive trace extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

Preferably, the first housing portion contacts the outer side surfaces of the chip and is spaced from the upper surface, and the second housing portion contacts the conductive trace and is spaced from the lower surface.

It is also preferred that the insulative housing includes top, bottom and peripheral side surfaces, the first housing portion provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface, and the second housing portion provides a central portion of the top surface.

It is also preferred that the peripheral portion of the top surface is shaped as a rectangular peripheral ledge with inner side surfaces opposite the peripheral side surfaces and outside a periphery of the chip, and the second housing portion is located within and recessed relative to the peripheral ledge.

It is also preferred that the first housing portion is a transfer molded material, and the second housing portion is a cured polymeric material.

It is also preferred that the conductive trace protrudes laterally from and extends through a peripheral side surface of the first housing portion, and the conductive trace includes a recessed portion that extends through the peripheral side surface and is spaced from the top and bottom surfaces and a non-recessed portion that extends outside the insulative housing and is adjacent to the recessed portion and a corner between the side surface and the top surface.

It is also preferred that the device is devoid of wire bonds, TAB leads and solder joints.

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In accordance with another aspect of the invention, a method of making an optoelectronic semiconductor package device includes attaching a conductive trace to a semiconductor chip using an insulative adhesive, wherein the chip includes a light sensitive cell and a conductive pad, forming a first single-piece insulative housing portion that contacts the chip and the

5   conductive trace without contacting the light sensitive cell, forming a connection joint that contacts and electrically connects the conductive trace and the pad, and forming a second insulative housing portion that contacts the first housing portion and the light sensitive cell and is transparent.

An advantage of the optoelectronic semiconductor package device of the present

10   invention is that it is reliable, cost-effective, easily manufacturable, and can be directly mounted on a printed circuit board. Another advantage is that the device need not include wire bonds, TAB leads or solder joints. Another advantage is that the first housing portion can surround and interlock the conductive traces. Another advantage is that the second housing portion can provide a compact, low cost optical window. Another advantage is that the device can be

15   manufactured using low temperature processes which reduces stress and improves reliability. A further advantage is that the device can be manufactured using well-controlled processes which can be easily implemented by circuit board, lead frame and tape manufacturers. Still another advantage is that the device can be manufactured using materials that are compatible with copper chip and lead-free environmental requirements.

20   These and other objects, features and advantages of the invention will be further described and more readily apparent from a review of the detailed description of the preferred embodiments which follows.

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BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description of the preferred embodiments can best be understood when read in conjunction with the following drawings, in which:

FIGS. 1A-14A are bottom perspective views that show a method of making an optoelectronic semiconductor package device in accordance with an embodiment of the present invention;

FIGS. 1B-14B are top perspective views corresponding to FIGS. 1A-14A, respectively;

FIGS. 2C, 2D and 2E are enlarged cross-sectional views taken across line 2C—2C in FIGS. 2A and 2B that show the formation of a representative slot in greater detail;

FIGS. 2F, 2G and 2H are enlarged cross-sectional views taken across line 2F—2F in FIGS. 2A and 2B that show the formation of a representative recessed portion in greater detail;

FIGS. 3C, 3D and 3E are enlarged cross-sectional views taken across line 3C—3C in FIG. 3A that show the formation of a representative metal trace in greater detail;

FIG. 4C is an enlarged cross-sectional view taken across line 4C—4C in FIG. 4A that shows the liquid resin on a representative metal trace in greater detail;

FIG. 5C is an enlarged plan view of encircled detail 5C in FIG. 5A that shows a representative pad and metal trace in greater detail;

FIG. 6C is an enlarged cross-sectional view taken across line 6C—6C in FIG. 6A that shows the encapsulant filling a representative slot in greater detail;

FIG. 6D is an enlarged cross-sectional view taken across line 6D—6D in FIG. 6A that shows the encapsulant filling a representative recessed portion in greater detail;

FIG. 7C is an enlarged cross-sectional view taken across line 7C—7C in FIG. 7A that shows the encapsulant removed from a portion of a representative slot in greater detail;

FIG. 7D is an enlarged cross-sectional view taken across line 7D—7D in FIG. 7A that shows the encapsulant intact in a representative recessed portion in greater detail;

FIGS. 8C, 8D and 8E are enlarged cross-sectional views taken across line 8C—8C in FIG. 8B that show the formation of a protective coating in greater detail;

FIG. 10C is an enlarged perspective view of encircled detail 10C in FIG. 10B that shows a representative pad, metal trace and opening in greater detail;

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FIGS. 10D and 10E are enlarged cross-sectional views taken across lines 10D—10D and 10E—10E, respectively, in FIG. 10C;

FIG. 11C is an enlarged perspective view of encircled detail 11C in FIG. 11B that shows a representative pad, metal trace, opening and connection joint in greater detail;

FIGS. 11D and 11E are enlarged cross-sectional views taken across lines 11D—11D and 11E—11E, respectively, in FIG. 11C; and

FIG. 12C is an enlarged cross-sectional view taken across line 12C—12C in FIG. 12B that shows the transparent base in greater detail.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. 1A-14A and 1B-14B are bottom and top perspective views, respectively, of a method of making an optoelectronic semiconductor package device in accordance with an embodiment of the present invention.

5   FIGS. 1A and 1B are bottom and top perspective views, respectively, of semiconductor chip 110 which is an integrated circuit in which various transistors, circuits, interconnect lines and the like are formed (not shown). Chip 110 is an optoelectronic image sensor that converts light into electronic signals. Chip 110 includes opposing major surfaces 112 and 114 and has a thickness of 200 microns between these surfaces. Surface 112 is an upper surface, and surface

10   114 is a lower surface. Surface 112 is the active surface and includes light sensitive cell 115, conductive pads 116 and passivation layer 118. Light sensitive cell 115 is located at a central portion of surface 112, and pads 116 are spaced from light sensitive cell 15 and located at a peripheral portion of surface 112 near the outer side surfaces (or edges) of chip 110 between surfaces 112 and 114. Light sensitive cell 115 and pads 116 are substantially aligned with

15   passivation layer 118. Alternatively, if desired, light sensitive cell 115 and/or pads 116 can extend above or be recessed below passivation layer 118.

Light sensitive cell 115 is a vision cell designed to receive visible light from the external environment during normal operation of chip 110. Light sensitive cell 115 comprises an array of tiny photosensor elements (not shown) that convert the light energy incident upon them into

20   electrical signals.

Pads 116 provides bonding sites to electrically couple chip 110 with external circuitry. Thus, a particular pad 116 can be input/output pad or a power/ground pad. Pads 116 have a length and width of 70 microns.

Pads 116 have aluminum bases that are cleaned by dipping chip 110 in a solution

25   containing 0.05 M phosphoric acid at room temperature for 1 minute and then rinsed in distilled water. Thereafter, pads 116 are treated to provide surface layers that will accommodate subsequently formed connection joints. Pads 116 can be treated by depositing several metal layers, such as chromium/copper/gold or titanium/nickel/gold on the aluminum bases. The chromium or titanium layer provides a barrier for the aluminum base and an adhesive between

30   the overlaying metal and the aluminum base. The metal layers, however, are typically selectively deposited by evaporation or electroplating using a mask which is a relatively

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complicated process. Alternatively, pads 116 can be treated by forming nickel surface layers on the aluminum bases. For instance, chip 110 is dipped in a zinc solution to deposit a zinc layer on the aluminum bases. This step is commonly known as zincation. Preferably, the zinc solution contains about 150 grams/liter of NaOH, 25 grams/liter of ZnO, and 1 gram/liter of $NaNO_3$, as

5   well as tartaric acid to reduce the rate at which the aluminum bases dissolve. Thereafter, nickel surface layers are electrolessly deposited on the zincated aluminum bases. A suitable electroless nickel plating solution is Enthone Enplate NI-424 at 85°C.

FIGS. 2A and 2B are bottom and top perspective views, respectively, of metal base 120. Metal base 120 is a copper lead frame that includes opposing major surfaces 122 and 124, central

10   portion 126, slots 128, recessed portions 132 and 134, non-recessed portions 136 and leads 138. Slots 128 are formed in two parallel rows and extend between surfaces 122 and 124. Recessed portions 132 are formed in surface 124, extend into metal base 120 towards surface 122, and are between and adjacent to slots 128 in the same row. Recessed portions 134 are formed in surface 124, extend into metal base 120 towards surface 122, and are between and adjacent to slots 128

15   in separate rows. Non-recessed portions 136 are between and adjacent to slots 128 in the same row, and are adjacent to recessed portions 132. Leads 138 include recessed portions 132 and non-recessed portions 136.

Thus, recessed portions 132 and 134 are coplanar with non-recessed portions 136 at surface 122 and recessed relative to non-recessed portions 136 at surface 124. Leads 138 are

20   arranged in two parallel rows, include opposing parallel outer edges defined by adjacent slots 128, and the outer edges extend across recessed portions 132 and non-recessed portions 136. The combination of slots 128, recessed portions 132 and recessed portions 134 provide a continuous rectangular channel that is adjacent to and extends 360 degrees around central portion 126, and slots 128 provide comb-like canals that extend outwardly from the channel. Metal base 120

25   includes other openings and notches that are used for tooling engagement and alignment purposes.

Metal base 120 has a thickness of 200 microns, slots 128 have a length of 1500 microns, a width of 300 microns and a center-to-center spacing of 800 microns, recessed portions 132 have a length and width of 500 microns and a depth of 120 microns, recessed portions 134 have a

30   width of 500 microns and a depth of 120 microns, and leads 138 have a length of 1500 microns

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(500 microns at recessed portions 132 and 1000 microns at non-recessed portions 136), a width of 500 microns and a center-to-center spacing of 800 microns.

FIGS. 2C, 2D and 2E are enlarged cross-sectional views taken across line 2C—2C in FIGS. 2A and 2B that show the formation of a representative slot 128 in greater detail, and

5 FIGS. 2F, 2G and 2H are enlarged cross-sectional views taken across line 2F—2F in FIGS. 2A and 2B that show the formation of a representative recessed portion 132 in greater detail.

FIGS. 2C and 2F are enlarged cross-sectional views of photoresist layers 142 and 144 formed on surfaces 122 and 124, respectively. Photoresist layers 142 and 144 are simultaneously deposited as continuous dry films and then patterned by selectively applying light through

10 respective reticles (not shown), applying a developer solution to remove the photoresist portions rendered soluble by the light, and then hard baking, as is conventional. As a result, photoresist layer 142 contains openings that selectively expose portions of surface 122, and photoresist layer 144 contains openings that selectively expose portions of surface 124. Photoresist layers 142 and 144 have a thickness of 15 microns.

15 FIGS. 2D and 2G are enlarged cross-sectional views of various features formed in metal base 120 by wet chemical etching using photoresist layers 142 and 144 as etch masks. In particular, the structure is dipped in a wet chemical etch that provides a front-side etch through the openings in photoresist layer 142 to the exposed portions of surface 122 and a back-side etch through the openings in photoresist layer 144 to the exposed portions of surface 124. The

20 structure is submerged in the wet chemical etch long enough for the etchant to etch about 120 microns into metal base 120. That is, the wet chemical etch provides a "half-etch" that removes slightly over one-half (120/200) the thickness of metal base 120 at the exposed portions. Thus, the front-side etch partially forms slot 128, the back-side etch partially forms slot 128 and completely forms recessed portion 132, and the combination of the front-side and back-side

25 etches completely forms slot 128. Likewise, the front-side and back-side etches are applied simultaneously, and slot 128 and recessed portion 132 are formed simultaneously. The wet chemical etch also forms the other slots 128 and recessed portions 132 as well as recessed portions 134 and the unlabeled openings and notches in a similar manner.

A suitable wet chemical etch can be provided by a solution containing alkaline ammonia,

30 sulfuric acid with hydrogen peroxide, chromic-sulfuric acid, phosphoric acid with ammonium

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persulfate, copper sulfate, copper chloride or ferric chloride. The optimal etch time for exposing metal base 120 to the wet chemical etch to provide the desired etch depth can be established through trial and error.

FIGS. 2E and 2H are enlarged cross-sectional views of metal base 120 after photoresist
5 layers 142 and 144 are simultaneously stripped.

FIGS. 3A and 3B are bottom and top perspective views, respectively, of metal traces 144 formed on metal base 120. Metal traces 144 extend to leads 138. More particularly, metal traces 144 extend from central portion 126 to recessed portions 132 where they are centered between the adjoining slots 128 but do not extend to non-recessed portions 136. Accordingly, leads 138
10 and metal traces 144 are formed in one-to-one relation. Conductive traces 150 include leads 138 and metal traces 144.

Metal traces 144 are electroplated onto metal base 120. Metal traces 144 are composed of a first nickel layer electroplated onto metal base 120, a copper layer electroplated onto the first nickel layer, and a second nickel layer electroplated onto the copper layer. Thus, the first nickel
15 layer is sandwiched between and contacts metal base 120 and the copper layer, the copper layer is sandwiched between and contacts the first and second nickel layers, and the second nickel layer contacts the copper layer and is exposed. The first and second nickel layers and the copper layer are shown as a single layer for convenience of illustration.

Metal traces 144 have a thickness of 10 microns provided by the first nickel layer with a
20 thickness of 1 micron, the copper layer with a thickness of 8 microns, and the second nickel layer with a thickness of 1 micron. Metal traces 144 have a width (orthogonal to the elongated length) of 55 microns.

FIGS. 3C, 3D and 3E are enlarged cross-sectional views taken across line 3C—3C in FIG. 3A that show the formation of a representative metal trace 144 in greater detail.

25 FIG. 3C is an enlarged cross-sectional view of photoresist layer 152 formed on surface 122. Photoresist layer 152 is deposited as a continuous dry film and then patterned by selectively applying light through a reticle (not shown), applying a developer solution to remove the photoresist portions rendered soluble by the light, and then hard baking, as is conventional. As a result, photoresist layer 152 contains an opening that selectively exposes a portion of surface
30 122. Photoresist layer 152 has a thickness of 15 microns.

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FIG. 3D is an enlarged cross-sectional view of metal trace 144 formed on metal base 120. Metal trace 144 is formed in the opening in photoresist layer 152 and on the exposed portion of surface 122 by an electroplating operation using photoresist layer 152 as a plating mask. Thus, metal trace 144 is formed additively. Initially, a plating bus (not shown) is connected to metal

5 base 120, current is applied to the plating bus from an external power source, and metal base 120 is submerged in an electrolytic nickel plating solution such as Technic Techni Nickel "S" at room temperature. As a result, the first nickel layer electroplates (deposits or grows) on the exposed portion of surface 122. The nickel electroplating operation continues until the first nickel layer has the desired thickness. Thereafter, the structure is removed from the electrolytic

10 nickel plating solution and submerged in an electrolytic copper plating solution such as Sel-Rex CUBATH M™ at room temperature while current is applied to the plating bus to electroplate the copper layer on the first nickel layer. The copper electroplating operation continues until the copper layer has the desired thickness. Thereafter, the structure is removed from the electrolytic copper plating solution and submerged in an electrolytic nickel plating solution such as Technic

15 Techni Nickel "S" at room temperature while current is applied to the plating bus to electroplate the second nickel layer on the copper layer. The nickel electroplating operation continues until the second nickel layer has the desired thickness. Thereafter, the structure is removed from the electrolytic nickel plating solution and rinsed in distilled water to remove contaminants.

FIG. 3E is an enlarged cross-sectional view of metal base 120 and metal trace 144 after

20 photoresist layer 152 is stripped.

FIGS. 4A and 4B are bottom and top perspective views, respectively, of transparent adhesive 154 formed on metal base 120 and metal traces 144. Transparent adhesive 154 is initially clear TEFLON® synthetic polymeric resin (polytetrafluoroethylene) from E.I. Dupont Chemical Company. The liquid resin is applied over a predetermined portion of central portion

25 126 using stencil printing. During stencil printing, a stencil (not shown) is placed over metal base 120, a stencil opening is aligned with the predetermined portion, and then a squeegee (not shown) pushes the liquid resin along the surface of the stencil opposite metal base 120, through the stencil opening and onto the predetermined portion. The liquid resin is compliant enough at room temperature to conform to virtually any shape. The predetermined portion of central

30 portion 126 is slightly offset from the periphery of central portion 126. Therefore, the liquid

resin does not reach surface 124 or slots 128. The liquid resin has a thickness of 30 microns over surface 122.

FIG. 4C is an enlarged cross-sectional view taken across line 4C—4C in FIG. 4A that shows the liquid resin on a representative metal trace 144 in greater detail.

5   FIGS. 5A and 5B are bottom and top perspective views, respectively, of chip 110 mechanically attached to metal base 120 by transparent adhesive 154. Transparent adhesive 154 is disposed between and contacts surface 112 of chip 110 and metal base 120, and is disposed between and contacts surface 112 of chip 110 and metal traces 144. Thus, surface 112 of chip 110 faces towards metal base 120 and metal traces 144 and is covered, and surface 114 of chip

10   110 faces away from metal base 120 and metal traces 144 and is exposed. Chip 110 and metal base 120 do not contact one another, and chip 110 and metal traces 144 do not contact one another.

Chip 110 and metal base 120 are positioned relative to one another so that chip 110 is disposed within the periphery of transparent adhesive 154, metal traces 144 extend within and

15   outside the periphery of chip 110 and overlap and are electrically isolated from pads 116, and slots 128, recessed portions 132 and 134, non-recessed portions 136 and leads 138 are disposed outside the periphery of chip 110. Metal traces 144 overlap pads 116 in one-to-one relation. Thus, each pad 116 has an associated conductive trace 150 which includes a single lead 138 and metal trace 144.

20   Chip 110 and metal base 120 can be aligned using an automated pattern recognition system. Transparent adhesive 154 is sandwiched between chip 110 and metal base 120 using relatively low pressure. Thereafter, transparent adhesive 154 is heated and fully cured at relatively low temperature of about 150°C to form a solid adhesive transparent electrically insulative die attach that mechanically fastens chip 110 to metal base 120 and metal traces 144.

25   Transparent adhesive 154 is 10 microns thick between pads 116 and metal traces 144.

At this stage, metal base 120 provides a carrier for chip 110, and transparent adhesive 154 contacts and covers light sensitive cell 115 and pads 116.

FIG. 5C is an enlarged plan view of encircled detail 5C in FIG. 5A that shows a representative pad 116 and metal trace 144 in greater detail. Since pad 116 and metal trace 144

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are not be visible from surface 114 of chip 110, they are shown in phantom. Metal trace 144 includes a distal end that overlaps pad 116.

FIGS. 6A and 6B are bottom and top perspective views, respectively, of encapsulant 156 formed on chip 110 and metal base 120 by transfer molding. Transfer molding is the most

5   popular chip encapsulation method for essentially all plastic packages. Generally speaking, transfer molding involves forming components in a closed mold from a molding compound that is conveyed under pressure in a hot, plastic state from a central reservoir called the transfer pot through a tree-like array of runners and gates into closed cavities. Molding compounds are well-known in the art.

10   Initially the structure is accurately positioned within a mold (not shown). The mold contacts surfaces 122 and 124 slightly outside recessed portions 132 and 134, but does not contact or extend into recessed portions 132 and 134. The mold defines a box-shaped mold cavity that extends above surface 122, surrounds chip 110 and transparent adhesive 154, overlaps recessed portions 132 and 134, and slightly overlaps non-recessed portions 136. Thus, portions

15   of slots 128 adjacent to recessed portions 132 extend into the mold cavity, while other portions of slots 128 adjacent to non-recessed portions 136 do not. Next, encapsulant 156 is introduced into the mold cavity as a liquid resin under pressure and then hardened to form a solid single-piece non-transparent molded plastic base during the transfer molding operation. Encapsulant 156 fills the mold cavity and contacts all exposed surfaces within the mold cavity. As a result,

20   encapsulant 156 forms a box-shaped portion, shaped like the mold cavity, that contacts and extends above surface 114 and the outer side surfaces of chip 110, surface 122, metal traces 144 and transparent adhesive 154. Furthermore, encapsulant 156 fills slots 128 and recessed portions 132 and 134. That is, since slots 128 and recessed portions 132 and 134 form a continuous rectangular channel with outwardly extending comb-like canals, and encapsulant 156 enters slots

25   128 and recessed portions 132 and 134 under pressure, encapsulant 156 fills and assumes the shape of the channel and canals. However, surface 124 outside recessed portions 132 and 134 remains exposed, and encapsulant 156 does not contact (or contacts substantially none of) surface 124 outside recessed portions 132 and 134. Likewise, encapsulant 156 does not contact light sensitive cell 115 or pads 116.

30   Encapsulant 156 forms a first single-piece housing portion that includes bottom surface 160, four peripheral side surfaces 162 and top surface 164. Encapsulant 156 also includes

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peripheral portion 166 at top surface 164. Peripheral portion 166 has a rectangular shape (in the channel) with outwardly extending comb-like fingers (in the canals). Bottom surface 160 occupies the entire surface area between side surfaces 162, however top surface 164 does not. Peripheral portion 166 occupies a peripheral portion of the surface area between side surfaces

5   162 that is outside the periphery of chip 110 without occupying an inner central portion of the surface area between side surfaces 162. Central portion 126 is surrounded by, adjacent to and coplanar with peripheral portion 166, occupies the inner central portion and remains exposed. Thus, top surface 164 of encapsulant 156 at peripheral portion 166 is coplanar with surface 124 of metal base 120 at central portion 126. In addition, encapsulant 156 completely surrounds

10 leads 138. In particular, encapsulant 156 contacts the bottoms of recessed portions 132 at surface 122, the outer edges of recessed portions 132 at slots 128, and the tops of recessed portions 132 at surface 124, thereby forming lateral openings with sidewalls that contact and span 360 degrees around leads 138. As a result, encapsulant 156 interlocks leads 138, thereby enhancing the mechanical attachment between chip 110 and leads 138.

15   Encapsulant 156 is a solid adherent compressible protective layer that provides back-side environmental protection such as moisture resistance and particle protection for chip 110 as well as mechanical support for leads 138.

        FIG. 6C is an enlarged cross-sectional view taken across line 6C—6C in FIG. 6A that shows encapsulant 156 filling a representative slot 128 in greater detail, and **FIG. 6D** is an

20 enlarged cross-sectional view taken across line 6D—6D in FIG. 6A that shows encapsulant 156 filling a representative recessed portion 132 in greater detail.

        FIGS. 7A and **7B** are bottom and top perspective views, respectively, of encapsulant 156 removed from portions of slots 128 that laterally extend outwardly at side surfaces 162. In other words, the comb-like fingers of encapsulant 156 are selectively removed while the remainder of

25 encapsulant 156 remains intact. This can be accomplished using a mechanical trimming operation. For instance, a mold die (not shown) with an excise blade and a base can be used. The excise blade contains two rows of comb-like blade portions that are aligned with and disposed above slots 128, and the base contains two rows of openings that are aligned with and disposed below slots 128 as the structure is spaced from the excise blade and rests on the base.

The excise blade is then actuated toward the base such that each blade portion enters a corresponding slot 128 and cuts off the finger of encapsulant 156 within that slot.

At this stage, leads 138 are arranged in opposing rows that protrude laterally from and extend through two opposing side surfaces 162 of encapsulant 156.

5   FIG. 7C is an enlarged cross-sectional view taken across line 7C—7C in FIG. 7A that shows encapsulant 156 removed from a portion of a representative slot 128 in greater detail, and FIG. 7D is an enlarged cross-sectional view taken across line 7D—7D in FIG. 7A that shows encapsulant 156 intact in a representative recessed portion 132 in greater detail.

FIGS. 8A and 8B are bottom and top perspective views, respectively, of protective

10   coating 170 formed on metal base 120 outside the periphery of encapsulant 156. Thus, protective coating 170 covers the exposed surfaces of metal base 120 outside central portion 126. More particularly, protective coating 170 covers the portions of leads 138 that protrude from encapsulant 156 as well as the remaining portions of metal base 120 outside leads 138. Protective coating 170 is electroplated onto metal base 120 and is composed of tin with a

15   thickness of 20 microns. For convenience of illustration, protective coating 170 is considered a surface layer that is part of metal base 120 and leads 138.

FIGS. 8C, 8D and 8E are enlarged cross-sectional views taken across line 8C—8C in FIG. 8B that show the formation of protective coating 170 in greater detail.

FIG. 8C is an enlarged cross-sectional view of ink layer 172 formed on surface 124. Ink

20   layer 172 is deposited as a liquid resin (A stage) epoxy over central portion 126 using stencil printing. Thereafter, the liquid resin is cured or hardened at relatively low temperature of about 120°C to form a solid layer. As a result, ink layer 172 covers central portion 126 at surface 124, overlaps encapsulant 156 at surface 164 and selectively exposes the remainder of metal base 120 outside encapsulant 156. Ink layer 172 has a thickness of 30 microns.

25   FIG. 8D is an enlarged cross-sectional view of protective coating 170 formed on metal base 120. Protective coating 170 is formed on the exposed portions of metal base 120 by an electroplating operation using ink layer 172 as a plating mask. Initially, a plating bus (not shown) is connected to metal base 120, current is applied to the plating bus from an external power source, and metal base 120 is submerged in an electrolytic tin plating solution such as

30   Technic Techni NF MTB at room temperature. As a result, the tin electroplates on the exposed

surfaces of metal base 120. The tin electroplating operation continues until the tin layer has the desired thickness. Thereafter, the structure is removed from the electrolytic tin plating solution and rinsed in distilled water to remove contaminants.

FIG. 8E is an enlarged cross-sectional view of metal base 120 and protective layer 170 after ink layer 172 is stripped using an alkaline solution that is highly selective of the epoxy ink with respect to tin, copper and the molding compound.

FIGS. 9A and 9B are bottom and top perspective views, respectively, of the structure after central portion 126 of metal base 120 is removed. The structure is dipped in a wet chemical etch that is highly selective of copper with respect to tin, nickel, the polymeric adhesive and the molding compound. Therefore, the wet chemical etch removes central portion 126 but has no appreciable effect on chip 110, leads 138, metal traces 144, transparent adhesive 154, encapsulant 156 and protective coating 170. As a result, metal traces 144 and transparent adhesive 154 become exposed. Peripheral portion 166 is shaped as a rectangular peripheral ledge with four inner side surfaces 174 previously adjacent to and covered by central portion 126 that become exposed. Inner side surfaces 174 are located within and face away from outer side surfaces 162, are orthogonal to top surface 164, and extend between transparent adhesive 154 and top surface 164.

A suitable wet chemical etch can be provided by the same solution used to form slots 128 and recessed portions 132 and 134. The optimal etch time for exposing the structure to the wet chemical etch without excessively exposing the portions of leads 138 embedded in peripheral portion 166 and adjacent to inner side surfaces 174 the selected copper has been removed can be established through trial and error.

The wet chemical etch removes central portion 126 and reaches metal traces 144 and transparent adhesive 154. However, the first nickel layers of metal traces 144, which were electroplated on metal base 120, become the exposed surface layers for metal traces 144. Furthermore, metal traces 144 are embedded in and coplanar with transparent adhesive 154 at the exposed surface that was adjacent to central portion 126. Therefore, the exposed nickel surfaces of metal traces 144 and transparent adhesive 154 provide etch masks that protect the underlying copper layers (between the first and second nickel layers) of metal traces 144.

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Advantageously, encapsulant 156 interlocks and provides mechanical support for leads 138, and therefore reduces the mechanical strain on transparent adhesive 154. The enhanced mechanical strength is particularly useful after central portion 126 has been removed.

At this stage, chip 110 remains embedded in transparent adhesive 154 and encapsulant 156, metal traces 144 overlap and remain electrically isolated from pads 116, and light sensitive cell 115 is visible through transparent adhesive 154.

FIGS. 10A and 10B are bottom and top perspective views, respectively, of the structure after portions of transparent adhesive 154 are selectively removed to form openings 176 in transparent adhesive 154 that expose pads 116. Openings 176 are formed by applying a suitable etch that is highly selective of transparent adhesive 154 with respect to pads 116 and metal traces 144.

In this instance, a selective laser etch is applied. Using projection laser ablation, a metal mask (not shown) is positioned relative to transparent adhesive 154 such that openings in the metal mask are aligned with pads, and a laser is directed to the side of the metal mask opposite transparent adhesive 154. Accordingly, the metal mask targets the laser at pads 116. The laser removes portions of transparent adhesive 154 above pads 116 and outside metal traces 144. Openings 176 have a diameter of 100 microns, and pads 116 (with a length and width of 70 microns) are exposed by and axially aligned with openings 176. Metal traces 144 shield the underlying transparent adhesive 154 from the laser etch so that the portions of transparent adhesive 154 sandwiched between metal traces 144 and pads 116 remain intact. Openings 176 are formed in transparent adhesive 154 without damaging pads 116, passivation layer 118 and metal traces 144. Thus, openings 176 extend through transparent adhesive 154, but do not extend into chip 110.

FIG. 10C is an enlarged perspective view of encircled detail 10C in FIG. 10B that shows a representative pad 116, metal trace 144 and opening 176 in greater detail, and FIGS. 10D and 10E are enlarged cross-sectional views taken across lines 10D—10D and 10E—10E, respectively, in FIG. 10C.

FIGS. 11A and 11B are bottom and top perspective views, respectively, of connection joints 180 formed on pads 116 and metal traces 144 by ball bonding.

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Connection joints 180 are formed in openings 176 and contact pads 116 and metal traces 144, thereby electrically connecting pads 116 and metal traces 144. Connection joints 180 are composed of gold and are formed by thermosonic wire bonding. Preferably, the regions of pads 116 and metal traces 144 that are within or exposed by openings 176 are spot plated with silver

5   having a thickness 3 microns. Silver is particularly well-suited for receiving a gold ball bond connection joint, and the nickel between the silver and the copper prevents the formation of brittle silver-copper intermetallic compounds. Thereafter, a capillary with a gold wire ball is positioned above opening 176, the capillary moves downward such that the wire ball enters opening 176 and contacts pad 116 and metal trace 144 while the capillary is heated to about 150

10   to 200°C, and the capillary exerts a downward force of about 25 to 45 grams and provides horizontal ultrasonic oscillatory motions with a frequency of about 60 to 120 kHz. The combination of heat, pressure and ultrasonic vibration places the wire ball in a soft state which is easy to deform and forms a ball bond that contacts and is metallurgically bonded to pad 116 and metal trace 144. Thereafter, the capillary moves upward and away from the ball bond without

15   exerting upward pressure on the ball bond, and the ball bond cools and solidifies. The solidified ball bond forms connection joint 180 and the capillary moves in a horizontal loop and then downward with a force of 70 to 90 grams to cut the gold wire from connection joint 180. The process is repeated to form other connection joints 180 for corresponding pairs of pads 116 and metal traces 144.

20   Connection joints 180 are formed in openings 176 and contact and electrically connect pads 116 with metal traces 144. Connection joints 180 contact and cover portions of pads 116 beneath openings 176 and outside metal traces 144, the surfaces of metal traces 144 that overlap and face away from pads 116, and the outer edges (or three peripheral sidewalls) of metal traces 144 that overlap and are orthogonal to pads 116. Thus, connection joints 180 provide robust,

25   permanent electrical connections between pads 116 and metal traces 144.

Connection joints 180 are the only electrical conductors external to chip 110 that contact pads 116, transparent adhesive 154 and connection joints 180 are the only materials external to chip 110 that contact pads 116, and transparent adhesive 154 and connection joints 180 are the only materials that contact both pads 116 and metal traces 144.

30   FIG. 11C is an enlarged perspective view of encircled detail 11C in FIG. 11B that shows a representative pad 116, metal trace 144, opening 176 and connection joint 180 in greater detail,

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and **FIGS. 11D** and **11E** are enlarged cross-sectional views taken across lines 11D—11D and 11E—11E, respectively, in FIG. 11C.

FIGS. 12A and **12B** are bottom and top perspective views, respectively, of transparent base 182 disposed on the structure. Transparent base 182 is initially clear TEFLON® synthetic polymeric resin (polytetrafluoroethylene). The polymeric resin is deposited on the exposed portions of chip 110, metal traces 144, transparent adhesive 154 and connection joints 180 using stencil printing. The polymeric resin is compliant enough at room temperature to conform to virtually any shape, and therefore fills the remaining space in openings 176. Thereafter, the polymeric resin is cured or hardened at a relatively low temperature of about 150°C to form transparent base 182 as a solid single-piece transparent polymeric layer.

Transparent base 182 is disposed directly above light sensitive cell 115. Furthermore, transparent adhesive 154 and transparent base 182 are optically clear to visible light. Therefore, transparent adhesive 154 and transparent base 182 provide an optical window for light sensitive cell 115. Visible light from the external environment that impinges upon transparent base 182 passes through transparent base 182, impinges upon transparent adhesive 154, passes through transparent adhesive 154 and impinges upon light sensitive cell 115.

Transparent base 182 has a planar top surface and a thickness of 50 microns relative to transparent adhesive 154. Transparent base 182 contacts portions of inner side surfaces 174 adjacent to transparent adhesive 154 and covers the entire surface area formerly occupied by central portion 126. As a result, encapsulant 156 and transparent base 182 in combination form insulative housing 184 that surrounds and encapsulates chip 110. Insulative housing 184 includes top surface 164 formed by peripheral portion 166 and transparent base 182. Thus, peripheral portion 166 forms a rectangular peripheral ledge of top surface 164, and transparent base 182 forms a recessed central portion of top surface 164. Peripheral portion 166 protrudes 150 microns (200–50) above transparent base 182. However, transparent base 182 forms a central portion of top surface 164 of insulative housing 184 even though peripheral portion 166 forms a peripheral ledge of top surface 164 that protrudes above transparent base 182.

FIG. 12C is an enlarged cross-sectional view taken across line 12C—12C in FIG. 12B that shows transparent base 182 in greater detail.

FIGS. 13A and 13B are bottom and top perspective views, respectively, of the structure after metal base 120 outside leads 138 and insulative housing 184 is removed. In other words, metal base 120 is selectively cut to remove all portions of metal base 120, except for leads 138, outside insulative housing 184, while leads 138 and insulative housing 184 remain intact. This can be accomplished using an excise blade that selectively cuts metal base 120 at predetermined regions adjacent to leads 138 and insulative housing 184. As a result, optoelectronic semiconductor package device 186 is singulated from the lead frame.

At this stage, device 186 includes chip 110, conductive traces 150, transparent adhesive 154, connection joints 180 and insulative housing 184. Conductive traces 150 each include a lead 138 that protrudes laterally from extends through a side surface 162 of insulative housing 184, and a metal trace 144 within insulative housing 184 that contacts an associated lead 138 and connection joint 180. Conductive traces 150 are electrically connected to pads 116 by connection joints 180 in one-to-one relation, and are electrically isolated from one another. Leads 138 are arranged in opposing rows that protrude laterally from and extend through opposing side surfaces 162 and are disposed between top surface 164 and bottom surface 160. Furthermore, light sensitive cell 115 is protected by and exposed to incident light from the external environment by transparent adhesive 154 and transparent base 182.

FIGS. 14A and 14B are bottom and top perspective views, respectively, of device 186 after leads 138 are bent. Leads 138 are bent at inner corners 138A and outer corners 138B using a conventional lead forming tool. As a result, leads 138 include inner lateral portions 138C between inner corners 138A and insulative housing 184, vertical portions 138D between corners 138A and 138B, and outer lateral portions 138E between outer corners 138B and distal ends 138F. Lateral portions 138C and 138E are parallel to bottom surface 160 and parallel to one another. Vertical portions 138D are sloped and extend laterally away from inner lateral portions 138C with increasing vertical distance from inner lateral portions 138C. Outer lateral portions 138E are disposed beneath bottom surface 160. Thus, the lead bending operation moves distal ends 138F from between top surface 164 and bottom surface 160 to outside top surface 164 and bottom surface 160 such that distal ends 138F extend vertically beyond insulative housing 184. Furthermore, the lead bending operation converts leads 138 from straight planar leads to gullwing-shaped leads and device 186 becomes a thin small outline package (TSOP).

The optoelectronic semiconductor package device described above is merely exemplary. Numerous other embodiments are contemplated.

The light sensitive cell can include a wide variety of light sensitive elements designed to be selectively or continuously exposed to light in a selected frequency range during normal operation of the chip. For instance, the light sensitive cell can be designed to receive visible, ultraviolet or infrared light, combinations thereof, and selected frequencies thereof.

The pads can have numerous shapes including a flat rectangular shape and a bumped shape. For instance, a bump-shaped pad may extend into the opening and may even extend above the conductive trace. The pads can either be partially or completely exposed prior to forming the connection joints. The pads can have a length and width that are larger than, equal to, or smaller than the diameter of the openings. Preferably, the pads and openings have the same or similar size, and a substantial portion of the pads is directly beneath the openings.

The conductive traces can have various shapes and sizes. The conductive traces can overlap various portions of the pads, such as one peripheral edge and the center of the pad (FIG. 10C), two opposing peripheral edges and the center of the pad, three peripheral edges but not the center of the pad, two corners and the center of the pad, or four peripheral edges but not the center of the pad.

The conductive traces can be various conductive metals including copper, gold, nickel, aluminum, palladium, tin, combinations thereof, and alloys thereof. The preferred composition of the conductive traces will depend on the nature of the connection joints as well as design and reliability factors. Furthermore, those skilled in the art will understand that in the context of a semiconductor package device, a copper material is typically a copper alloy that is mostly copper but not pure elemental copper, such copper-zirconium (99.9% copper), copper-silver-phosphorus-magnesium (99.7% copper), or copper-tin-iron-phosphorus (99.7% copper). The conductive traces may function as a signal, power or ground layer depending on the purpose of the associated chip pads. Likewise, the conductive traces can fan-in, fan-out or both.

The metal traces can be a single layer or multiple layers. For instance, the metal trace can be a 5 micron layer of gold, or alternatively, a 4.5 micron layer of nickel electroplated on a 0.5 micron layer of gold electroplated on a copper base to reduce costs, or alternatively, a 4 micron layer of nickel electroplated on a 0.5 micron layer of gold electroplated on a 0.5 micron layer of tin electroplated on a copper base to reduce costs and avoid gold-copper alloys that may be

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difficult to remove when the copper base is etched. As another example, the metal trace can include a non-copper layer between a copper layer and the metal base. Suitable non-copper layers include nickel, gold, palladium and silver. After the metal trace is attached to the chip by the adhesive, a wet chemical etch can be applied that is highly selective of copper with respect to

5   the non-copper layer to remove the copper base without removing the copper or non-copper layers. The non-copper layer provides an etch stop that prevents the wet chemical etch from removing the copper layer. Furthermore, it is understood that in the context of the present invention, the metal trace and the metal base are different metals (or metallic materials) even if a multi-layer metal trace includes a single layer that is similar to the metal base (such as the

10   example described above).

The metal base can be various metals such as copper, gold, nickel, aluminum, palladium, tin, combinations thereof, and alloys thereof, and can be a single layer or multiple layers.

The metal base can be etched in numerous manners. For instance, portions of the metal base above the pads can be selectively etched to permit formation of the openings in the

15   adhesive, and other portions of the metal base can remain intact and connected to the conductive traces. Alternatively, portions of the metal base above the pads can be selectively etched to permit formation of the openings, and other portions of the metal base that are isolated from the conductive traces and disposed within the periphery of the chip can remain intact and provide heat sinks.

20   The transparent base can be a wide variety of optically clear materials including semi-transparent and substantially transparent materials. For instance, the transparent base can be a polymeric material such as polytetrafluoroethylene, water white clear epoxy, or EPO-TEK® 301 and 301-2FL from Epoxy Technology, Inc. that is deposited on the structure and then cured to form a solid adherent layer. Alternatively, the transparent base can be a solid cover, such as

25   borosilicate glass, plastic, polycarbonate or quartz that is deposited on the structure as a solid layer and attached to the structure using an adhesive. In either case, the transparent base can contact or be spaced from the light sensitive cell. Preferably, the transparent base is optically clear to the selected frequencies of light that the light sensitive cell is designed to sense so that the selected frequencies of light from the external environment that impinge upon the transparent

base pass through the transparent base with little or no attenuation or distortion and impinge upon the light sensitive cell.

The adhesive can be applied between the chip and the conductive trace in numerous manners. For instance, the adhesive can be applied as a paste, a laminated layer, or a liquid applied by screen-printing, spin-on, or spray-on. If paste or liquid adhesives are applied, the adhesive may contact the metal base, whereas if laminated adhesives are applied then no appreciable amount of adhesive may contact the metal base. Thermosetting adhesive liquids and pastes such as epoxies are generally suitable. Likewise, thermoplastic adhesives such as an insulative thermoplastic polyimide film with a glass transition temperature (Tg) of 400°C are also generally suitable.

The adhesive can be transparent or non-transparent. A transparent adhesive can be a wide variety of optically clear materials, including polymeric materials such as polytetrafluoroethylene, water white clear epoxy, EPO-TEK® 301 and 301-2FL from Epoxy Technology, Inc. and other semi-transparent and substantially transparent materials. Preferably, a transparent adhesive is optically clear to the selected frequencies of light that the light sensitive cell is designed to sense so that the selected frequencies of light from the external environment that impinge upon the transparent adhesive pass through the transparent adhesive with little or no attenuation or distortion and impinge upon the light sensitive cell.

A non-transparent adhesive can also be used. Preferably, a non-transparent adhesive does not contact or cover any portion of the light sensitive cell. For example, a non-transparent adhesive can be formed on the metal base as a peripheral ledge with a central opening, the chip can be positioned so that the non-transparent adhesive contacts the pads without contacting the light sensitive cell, and then the transparent base can be deposited on the light sensitive cell. As another example, a non-transparent adhesive can be deposited on the metal base, the chip can be positioned so that the non-transparent adhesive contacts the pads and the light sensitive cell, the portion of the non-transparent adhesive that contacts the light sensitive cell can be removed, for instance by selective laser ablation or blanket plasma etching as the pads are exposed, and then the transparent base can be deposited on the light sensitive cell.

The openings can be formed in the adhesive either before or after mechanically attaching the chip to the conductive traces. For instance, the adhesive can be applied as a liquid or paste

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(A stage) to the bottom surface of the conductive traces, the adhesive can be partially cured (B stage), a back-side etch can form the openings in the adhesive, the partially cured adhesive can be brought into contact with the chip, and then the adhesive can be fully cured (C stage). Alternatively, the liquid or paste adhesive can be sandwiched between the chip and the

5 conductive traces, the adhesive can be fully cured thereby mechanically fastening the chip to the conductive traces, and then a front-side etch can form the openings in the adhesive.

The openings can be formed with numerous etching techniques. For instance, the openings can be formed by laser direct write (without a mask) or a blanket plasma etch that removes portions of the adhesive not covered by the conductive traces. In addition, the openings

10 can have a circular, ovalar, square, rectangular or other shape. The openings may be aligned with and expose single pads or a plurality of pads. Furthermore, the openings can have sidewalls with a wide variety of shapes and slopes including vertical sidewalls, tapered sidewalls, continuous sidewalls and stepped sidewalls.

The encapsulant can be formed using a wide variety of techniques including printing and

15 transfer molding. For instance, the encapsulant can be an epoxy paste that is deposited and then cured or hardened. The encapsulant can be any of the adhesives mentioned above. Moreover, the encapsulant need not necessarily contact the chip. For instance, a glob-top coating can be deposited on the chip after mechanically attaching the chip to the conductive traces, and then the encapsulant can be formed on the glob-top coating.

20 The insulative housing can include a wide variety of insulative housing portions. For example, if a transparent adhesive contacts the light sensitive cell, and a transparent base contacts the transparent adhesive and is spaced from the light sensitive cell, then the encapsulant provides a first single-piece housing portion, the transparent base provides a second single-piece housing portion, the transparent adhesive provides a third single-piece housing portion, and the

25 transparent adhesive and transparent base provide an optical window for the light sensitive cell. As another example, if a non-transparent adhesive is spaced from the light sensitive cell, and a transparent base contacts the light sensitive cell, then the encapsulant provides a first single-piece housing portion, the transparent base provides a second single-piece housing portion, and the transparent base alone provides an optical window for the light sensitive cell. As another

30 example, if a transparent adhesive contacts the light sensitive cell, and the transparent base is omitted such that a side of the transparent adhesive opposite the chip is exposed, then the

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encapsulant provides a first single-piece housing portion, the transparent adhesive provides a second single-piece housing portion, and the transparent adhesive alone provides an optical window for the light sensitive cell.

The connection joints can be formed from a wide variety of materials including copper,
5   gold, nickel, palladium, tin, alloys thereof, and combinations thereof, can be formed by a wide variety of processes including electroplating, electroless plating, ball bonding, solder reflowing and conductive adhesive curing, and can have a wide variety of shapes as sizes. The shape and composition of the connection joints depends on the composition of the conductive traces as well as design and reliability considerations. Further details regarding an electroplated connection
10   joint are disclosed in U.S. Application Serial No. 09/865,367 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electroplated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding an electrolessly plated connection joint are disclosed in U.S. Application Serial No. 09/864,555 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with
15   Simultaneously Electrolessly Plated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding a ball bond connection joint are disclosed in U.S. Application Serial No. 09/864,773 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Ball Bond Connection Joint" which is incorporated by reference. Further details regarding a solder or conductive adhesive connection joint are
20   disclosed in U.S. Application Serial No. 09/927,216 filed August 10, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Hardened Connection Joint" which is incorporated by reference.

The conductive traces can be formed and attached to the chip by a wide variety of lead-on-chip (LOC) and other connection techniques. See, for instance, U.S. Application Serial No.
25   09/878,649 filed June 11, 2001 by Charles W.C. Lin entitled "Method of Making a Semiconductor Chip Assembly with a Conductive Trace Subtractively Formed Before and After Chip Attachment," U.S. Application Serial No. 09/878,626 filed June 11, 2001 by Charles W.C. Lin entitled "Method of Connecting a Conductive Trace to a Semiconductor Chip," U.S. Application Serial No. 09/939,140 filed August 24, 2001 by Charles W.C. Lin entitled
30   "Semiconductor Chip Assembly with Interlocked Conductive Trace," and U.S. Application Serial No. 09/962,754 filed September 24, 2001 by Charles W.C. Lin entitled "Method of

Connecting a Conductive Trace and an Transparent base to a Semiconductor Chip," each of which is incorporated by reference. Conventional wire bonding, TAB and flip-chip techniques can also be employed. With conventional wire bonding, TAB and flip-chip techniques, the connection joints between the conductive traces and the pads can be formed before the

5   encapsulant is formed.

The "upper" and "lower" surfaces of the chip and the "top" and "bottom" surfaces of the insulative housing do not depend on the orientation of the device, as will be readily apparent to those skilled in the art. For instance, the upper surface of the chip includes the light sensitive cell and the pads, regardless of whether the chip is inverted, and regardless of whether the device is

10   inverted and/or mounted on a printed circuit board. Similarly, the upper surface of the chip faces and is covered by the top surface of the insulative housing, and the lower surface of the chip faces and is covered by the bottom surface of the insulative housing, regardless of whether the device is inverted, rotated or slanted. Likewise, the device is shown with a single orientation throughout the drawings for ease of comparison between the figures, although the device may be

15   inverted at various manufacturing stages. For instance, the metal base should be inverted so that the bottom surface faces upward when the adhesive is deposited on the metal base.

The optoelectronic semiconductor package device of the present invention can have a wide variety of packaging formats as required by the next level assembly. For instance, the conductive traces can be configured so that the device is a surface mount technology (SMT)

20   package such as a small outline package (SOP), thin small outline package (TSOP), quad flat package (QFP), plastic leadless chip carrier (PLCC) or small outline J-lead package (SOJ). The conductive traces can also be configured so that the device is a through-hole package such as a dual in-line package (DIP), single in-line package (SIP) or zig-zag in-line package (ZIP). The conductive traces can also be configured so that the device is a grid array such as a ball grid array

25   (BGA), column grid array (CGA), land grid array (LGA) or pin grid array (PGA).

Advantageously, the optoelectronic semiconductor package device of the present invention is reliable and inexpensive. The encapsulant and the transparent base protect the chip from handling damage and provide a known dielectric barrier for the conductive traces. The encapsulant also provides critical mechanical support for the conductive traces after the metal

30   base is etched. The mode of the connection between the chip and the conductive traces shifts from the initial mechanical coupling to metallurgical coupling to assure sufficient metallurgical

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bond strength. Furthermore, the conductive traces can be mechanically and metallurgically coupled to the chip without wire bonding, TAB or solder joints, although the process is flexible enough to accommodate these techniques if desired. As a result, the device significantly enhances throughput, yield and performance characteristics compared to conventional packaging

5   techniques. Moreover, the device is well-suited for use with materials compatible with copper chip and lead-free environmental requirements.

Various changes and modifications to the presently preferred embodiments described herein will be apparent to those skilled in the art. For instance, the materials, dimensions and shapes described above are merely exemplary. Such changes and modifications may be made

10   without departing from the spirit and scope of the present invention as defined in the appended claims.